

# CONTENTS

PREFACE xi

## 1

### COMPUTER OPERATION 1

	1.1	Electronic Digital Computers	2
	1.2	Application of Computers to Problems	3
	1.3	Business Applications	5
	1.4	Scientific Applications	6
2 <sup>nd</sup> →	1.5	Some Different Types of Computer Systems	7
2 <sup>nd</sup> {	1.6	Computers in Control Systems	11
2 <sup>nd</sup> {	1.7	Basic Components of a Digital Computer	13
4 <sup>th</sup> {	1.8	Construction of Memory	14
	1.9	Instructions	15
5 <sup>th</sup> {	1.10	Multiplication Instruction	17
	1.11	Branch, Skip, or Jump Instructions	18
	1.12	Programming Systems	20
	1.13	Assembly Languages	21
6 <sup>th</sup> {	1.14	High-Level Languages	23
	1.15	A Short Introduction to Higher-Level Languages	23
	1.16	Summary	27

## 2 NUMBER SYSTEMS 33

2.1	Decimal System	34
2.2	Bistable Devices	35
2.3	Counting in the Binary System ✓	35
2.4	Binary Addition and Subtraction ✓	36
2.5	Binary Multiplication and Division ✓	37
2.6	Converting Decimal Numbers to Binary	39
2.7	Negative Numbers	40
2.8	Use of Complements to Represent Negative Numbers	41
2.9	Complements in Other Number Systems ✓	43
2.10	Binary Number Complements ✓	43
2.11	Binary-Coded-Decimal Number Representation ✓	44
2.12	Octal and Hexadecimal Number Systems ✓	46
2.13	Summary	51

## 3 BOOLEAN ALGEBRA AND GATE NETWORKS 59

3.1	Fundamental Concepts of Boolean Algebra	60
3.2	Logical Multiplication	61
3.3	AND Gates and OR Gates	62
3.4	Complementation and Inverters	63
3.5	Evaluation of Logical Expressions	65
3.6	Evaluation of an Expression Containing Parentheses	66
3.7	Basic Laws of Boolean Algebra	67
3.8	Proof by Perfect Induction	70
3.9	Simplification of Expressions	71
3.10	De Morgan's Theorems	71
3.11	Basic Duality of Boolean Algebra	72
3.12	Derivation of a Boolean Expression	73
3.13	Interconnecting Gates	76
3.14	Sum of Products and Product of Sums	77
3.15	Derivation of Product-of-Sums Expressions	78
3.16	Derivation of Three-Input-Variable Expression	80
3.17	NAND Gates and NOR Gates	82
3.18	The Map Method for Simplifying Expressions	84
3.19	Subcubes and Covering	88
3.20	Product-of-Sums Expressions—Don't-Cares	93
3.21	Design Using NAND Gates	95
3.22	Design Using NOR Gates	98
3.23	NAND-to-AND and NOR-to-OR Gate Networks	101
3.24	Wired OR and Wired AND Gates	107
3.25	PLAs and PALs	109
3.26	Example of a Design Using a PLA	116
3.27	Summary	119

**4**  
**LOGIC DESIGN 135**

**vii**  
**CONTENTS**

4.1	Flip-Flops	136
4.2	Transfer Circuits	138
4.3	Clocks	139
4.4	Flip-Flop Designs	142
4.5	Gated Flip-Flop	142
4.6	Master-Slave Flip-Flop	144
4.7	Shift Register	147
4.8	Binary Counter	148
4.9	BCD Counters	153
4.10	Integrated Circuits	155
4.11	Medium-, Large-, and Very Large Scale Integration	162
4.12	Counter Design	166
4.13	State Diagrams and State Tables	170
4.14	Design of a Sequential Magnitude Comparator	176
4.15	Comments—Mealy Machines	178
4.16	Programmable Arrays of Logic Cells	180
4.17	Summary	183

**5**  
**THE ARITHMETIC-LOGIC UNIT 193**

5.1	Construction of the ALU	194
5.2	Integer Representation	195
5.3	Binary Half-Adder	196
5.4	Full-Adder	197
5.5	A Parallel Binary Adder	198
5.6	Positive and Negative Numbers	200
5.7	Addition in the 1s Complement System	201
5.8	Addition in the 2s Complement System	203
5.9	Addition and Subtraction in a Parallel Arithmetic Element	204
5.10	Full-Adder Designs	208
5.11	Binary-Coded-Decimal Adder	210
5.12	Positive and Negative BCD Numbers	212
5.13	Addition and Subtraction in the 9s Complement System	214
5.14	Shift Operation	218
5.15	Basic Operations	219
5.16	Binary Multiplication	223
5.17	Decimal Multiplication	226
5.18	Division	227
5.19	Logical Operations	233
5.20	Multiplexers	235
5.21	High-Speed Arithmetic—Speeding up Addition	239

5.22	High-Speed Arithmetic—Parallel Multipliers	243
5.23	Floating-Point Number Systems	243
5.24	Performing Arithmetic Operations with Floating-Point Numbers	251
5.25	Summary	252

## 6

### THE MEMORY ELEMENT 261

6.1	Random-Access Memories	263
6.2	Linear-Select Memory Organization	265
6.3	Decoders	269
6.4	Dimensions of Memory Access	272
6.5	Connecting Memory Chips to a Computer Bus	277
6.6	Random-Access Semiconductor Memories	281
6.7	Static Random-Access Memories	284
6.8	Dynamic Random-Access Memories	286
6.9	Read-Only Memories	288
6.10	Magnetic Disk Memories	295
6.11	Flexible-Disk Storage Systems—The Floppy Disk	299
6.12	Magnetic Tape	302
6.13	Tape Cassettes and Cartridges	307
6.14	Magnetic Bubble and CCD Memories	310
6.15	Digital Recording Techniques	311
6.16	Return-to-Zero and Return-to-Bias Recording Techniques	312
6.17	Nonreturn-to-Zero Recording Techniques	314
6.18	Summary	316

## 7

### INPUT-OUTPUT DEVICES 323

7.1	Punched Tape	324
7.2	Tape Readers	326
7.3	Punched Cards	328
7.4	Card Readers	329
7.5	Alphanumeric Codes	330
7.6	Character Recognition	332
7.7	Output Equipment	334
7.8	Printers	335
7.9	Cathode-Ray-Tube Output Devices	340
7.10	Magnetic-Tape Output Offline Operation	341
7.11	Error-Detecting and Error-Correcting Codes	342
7.12	Keyboards	343
7.13	Terminals	348
7.14	Input-Output Devices for Systems with Analog Components	351
7.15	Digital-to-Analog Converters	352
7.16	Analog-to-Digital Converters—Shaft Encoders	355

7.17	Analog-to-Digital Converters	357
7.18	Flash Converters	359
7.19	Counter and Successive-Approximation Converters	362
7.20	Computer Data Acquisition Systems	366
7.21	Summary	371

**8****BUSES AND INTERFACES 379**

8.1	Interconnecting System Components	380
8.2	Interfacing—Buses	386
8.3	Bus Formats and Operation	390
8.4	Isolated and Memory-Mapped Input-Output	394
8.5	Interfacing a Keyboard	400
8.6	Program Control of Keyboard Interface	405
8.7	Interfacing a Printer	406
8.8	Interrupts in Input-Output Systems	409
8.9	A Standard Bus Interface	413
8.10	Summary	417

**9****THE CONTROL UNIT 421**

9.1	Construction of Instruction Word	422
9.2	Instruction Cycle and Execution Cycle Organization of Control Registers	425
9.3	Sequence of Operation of Control Registers	428
9.4	Controlling Arithmetic Operations	430
9.5	Typical Sequence of Operations	434
9.6	BRANCH, SKIP, or JUMP Instructions	437
9.7	SHIFT Instructions	440
9.8	Register Transfer Language	443
9.9	Microprogramming	446
9.10	Variations in Microprogramming Configurations	450
9.11	Summary	452

**10****COMPUTER ORGANIZATION 455**

10.1	Instruction Word Formats—Number of Addresses	457
10.2	Representation of Instructions and Data	459
10.3	Addressing Techniques	459
10.4	Direct Addressing	460
10.5	Immediate Addressing	463
10.6	Paging	465
10.7	Relative Addressing	466
10.8	Indirect Addressing	468
10.9	Indexed Addressing	470
10.10	Single-Address Computer Organization	472

<b>x</b>	10.11 A Single-Address Microprocessor	481
<b>CONTENTS</b>	10.12 6800 Microprocessor	496
	10.13 PDP-11	506
	10.14 8086 and 8088 Microprocessors	515
	10.15 68000 Microprocessor	520

## **APPENDIXES**

### **A**

CIRCUIT PRINCIPLES 539

### **B**

DIODE GATES 545

### **C**

TRANSISTOR-TRANSISTOR LOGIC 549

### **D**

EMITTER-COUPLED LOGIC 557

### **E**

METAL-OXIDE SEMICONDUCTOR CIRCUITS 563

### **F**

IIL CIRCUITS 569

### **G**

DAC IMPLEMENTATION 573

BIBLIOGRAPHY 575

ANSWERS TO SELECTED ODD-NUMBERED QUESTIONS 581

INDEX 603